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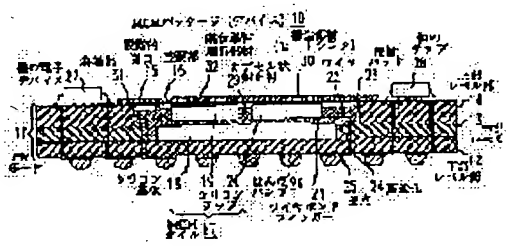
(54) MULTI-CHIP MODULE PACKAGE

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce the vertical dimension, that is, the thickness of a multichip module package by a method, wherein a cavity part is provided in a printed- wiring board to arrange efficiently an MCM tile in the cavity part.
SOLUTION: A silicon on silicon MCM tile 17, which consists of a silicon substrate 18 and silicon chips 19 and 20, is arranged in a cavity part 16 formed in a PW board 11, which has lower, middle and upper levels 12, 13 and 14. A wire-bonding finger 21 on the substrate 18 is interconnected with a contact pad 23 on the level part 13 of the board 11 via a wire 22. Whereupon, the cavity part 16 is sealed with a structural member. An adaptable capsule-shaped sealing material, which wraps the chips of the tile 17 therein, is made to fill the part 16. Thereby, the thickness of an MC package can be reduced, and a minimization of a system and a device, which adopt the package, becomes possible.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to mounting (packaging) of a semiconductor device which has the integrated-circuit unit applied to surface wearing (mounting) assembly.
[0002]
[Description of the Prior Art] The industrial use of portability and the product for consumers are in the inclination which miniaturizes size, lowers cost and increases functionality. From these requirements, many power points are placed by development of the semiconductor mounting technology which can hold large-scale and a more complicated integrated circuit in the smaller package in which the handling of bigger power density is possible more.
[0003] The conventional surface wearing (mounting) technology uses a plastic package with lead wire. However, while the lead-wire pitch and size of a plastic package with lead wire continue reduction, a problem like the badness of the solder assembly yield by the unsavoriness of control of the same smoothness of lead wire and the badness of the detailed pitch solder printing yield by reduction of a lead-wire pitch continuing will remain as a main important question point succeedingly.
[0004] One of the mounting methods considered to conquer these troubles is based on exaggerated mould plastics pad array carrier (following, OMPAC) technology. OMPAC assembly uses the laminate of the printed circuit board of a double-sided formula, or a printed wiring board. (A printed circuit board or a printed wiring board is hereafter called a printed wiring board or PW board)
[0005] Top metallic coating of PW board serves as a die pad for die installation of an integrated-circuit (IC) unit, and the grounding section from a wire bond finger. the multi chip module (MCM) tile with which IC unit has one semiconductor chip (die), many semiconductor chips, or at least one chip with which flip chip mounting was carried out on the silicon substrate -- since -- it becomes
[0006] A wire bond finger is prolonged to the method of outside to "the plated breakthrough" (the following, breakthrough) located near the marginal part of a package in PW board. The electrical continuity from the crowning side of PW board to a pars-basilaris-ossis-occipitalis side is obtained by the breakthrough. By carrying in a continuation the copper connection way plated from the breakthrough to the solder pad which is a solder heights (bump) trailer, a signalling channel is completed to the pars-basilaris-ossis-occipitalis side of PW board.
[0007] If a solder bump is removed, all the metallic circuit diagram forms on PW board are defined by the photograph means, it **********s and electroplating of them is carried out with copper, nickel, and gold. In order to interconnect IC unit on PW board, conventional epoxy die attachment and conventional wirebonding technology are used. Exaggerated molding processing of the PW board is carried out after a die and wirebonding using the conventional epoxy transition technology.
[0008] After post mould (after molding) curing, a package can prepare a solder bump and is examined electrically. The package obtained as a result calls a "ball grid array" (BGA) package. Since a BGA package is interconnected in a mother board further, for example, a solder bump is used.
[0009] A lot of other interconnection electric element whose mother boards generally have a far larger area than the BGA package of OMPAC, and cannot accumulate it easily on it at the chip or module like a capacitor, a transformer, and a resistor and the mounting IC and BGA of further others, a plug, and a connector are arranged.
[0010] the main advantages in comparison with the surface mounting technology with lead wire of the BGA package of OMPAC are that mounting interconnection density increased, that the yield of solder assembly is more high, and that there is no problem of the same smoothness of lead wire by having set the interval and having arranged the soldered-joint point uniformly, to the pars-basilaris-ossis-occipitalis side which is a package
[0011] Schematic drawing shows the cross section of the typical example 100 of the BGA (ball grid array) package of OMPAC (exaggerated mould plastics pad array carrier) by the conventional technology to drawing 11 . A package 100 (it is also hereafter called a device) has the IC unit 101. The IC unit 101 consists of a single die (chip) component in this example.
[0012] A device 100 has the printed wiring board (PW board) 102, and PW board has the molding compound 108 which seals the portion of the wire bond finger 103 which pastes up the polymer coating 104 on the wire bond finger 103 and the wire bond finger 103 which functions as a solder mask. The breakthrough [illegible] the copper pad 106 and a chip 101 on the wire 107 which interconnects the bond finger 103 and the chip 101 a[illegible] [illegible] four [illegible] contact pa[illegible] 6
[0013] The [illegible]

[0014],Schematic drawing shows the device 120 which is the modification of the BGA (ball grid array) package of OMPAC (exaggerated mould plastics pad array carrier) by the conventional technology to drawing 12 .
[0015] Here, the IC unit 121 is the module (a multi chip module (MCM) tile is called) 121 of a tile (silicon-on silicon) configuration which carried the silicon chip on the silicon substrate. the MCM tile 121 consists of chips 122 and 123 which are the plurality by which flip chip mounting was carried out to the interchange circuit on the silicon interconnection substrate 124 (not shown) with solder reflow technology
[0016] A silicon substrate 124 is mounted on the PW board 125, and the wire bond finger 126, the solder mask 127, a breakthrough 128, and the contact pad 129 are formed in the PW board 125. The interconnection of the silicon substrate 124 is carried out to the wire bond finger 126 by the wire 130. The protection shell 131 is filled up with a capsule-like sealing agent 132 like silicon gel which is highly adaptable, and this sealing agent protects the MCM tile 121. The solder bump 133 for finally interconnecting in a mother board (not shown) is formed in the contact pad 129.
[0017]
[Problem(s) to be Solved by the Invention] since a device 120 does not pass through the step of molding in contrast with a device 100 -- device assembly -- the severity of a molding process -- **** -- things are avoided However, it is desirable to cut down the thickness of a package. Furthermore, it is desirable for heat to be also efficiently removable from IC unit again.
[0018]
[Means for Solving the Problem] this invention mounts a semiconductor device like a-multi chip module (MCM) tile in various printing boards (PW board), and offers at least the package by new semiconductor device mounting from which the small package of size is obtained rather than the OMPAC device by the conventional technology in a perpendicular direction.
[0019] The MCM tile by this invention serves as an interconnection substrate which has the circumference metallic-coating section, at least one chip (IC), i.e., the integrated circuit, mounted on this substrate by solder reflow technology or electroconductive-glue technology. A printed wiring board (PW board) consists of the single level section or much level sections, and it has opening for holding at least one chip of an MCM tile in the interior.
[0020] Therefore, sizes differ in the kind of interconnection between a substrate and PW board, and this opening is larger than the substrate of an MCM tile about the interconnection of wirebonding, and smaller than the substrate of an MCM tile about the interconnection by the solder reflow or the electroconductive glue. In the case of the interconnection of wirebonding, an MCM tile is located in opening and located on the structure material which seals PW board or the end section of opening, or the front face of a heat sink. The other end of opening is release or is enclosed by a structural member, a heat sink, another PW board, or the mother board.
[0021] About the interconnection by the solder reflow or the electroconductive glue, opening is smaller than a substrate. And it is located and a chip and/or a substrate are located in opening so that opening may lap with the zone where the edge field of opening adjoins opening of PW board. The interconnection section is sealed with the capsule-like sealing agent which can adapt itself to altitude like silica gel.
[0022]
[Embodiments of the Invention] at least, in a perpendicular direction, size of this invention is smaller than the OMPAC device according the multi chip module (MCM) tile of silicon-on silicon to the conventional technology, it protects an MCM tile in efficiency, and has a heat sink for removing heat from an MCM tile -- the technology mounted in the form of a package and its package are offered
[0023] A common MCM tile serves as an interconnection substrate with solder reflow technology or electroconductive-glue technology, at least one chip (IC), i.e., the integrated circuit, mounted by the flip chip method on the substrate. A substrate is made from the various material which consists of silicon, a ceramic, and a plastics laminate. In order to make possible the interconnection of PW board of an MCM tile, or a mother board, circumference metallic coating is prepared on a substrate.
[0024] Below, it indicates about some modifications of mounting (this mounting) to PW board of the MCM tile by this invention. This mounting has attained size [compacter than mounting by the conventional technology of a kind as shown in drawing 11 and drawing 12 which can be contrasted with this mounting] at least with thinner thickness.
[0025] Opening for forming the cavernous section which locates an MCM tile in the interior is prepared, and after PW board is filled up with the capsule-like sealing agent with which the cavernous section has adaptability in cavernous circles, you make it located in it about an MCM tile, in each modification indicated below, so that the interconnection section between a chip and a substrate and the interconnection section between a substrate and PW board may be protected from environment.
[0026] In order to enable efficient removal of heat energy combining device mounting of a low form which has high-power density, the structural member which acts as a heat sink is prepared in a package, and it constitutes so that this structural member may seal the cavernous section and an MCM tile may be protected further. The heat absorbed with the heat sink is the well-known method technically, and is radiated. This can realize a heat sink top by [like air] carrying out a fluid circulation fault.
[0027] Removal of heat is further strengthened by contacting a thermal diffusion machine like for example, a heat spreader with a fin to a heat sink, and forming it. This thermal diffusion machine is cooled by the above fluid styles.
[0028] this invention relates to attaining the minimum possible vertical (perpendicular) size combining the structural member which includes the way (****) and/or heat sink function which miss heat outside and which has been arranged the optimal.
However [illegible] uses without the [illegible] that originally [illegible] uses a heat sink [illegible] **** for a low sake exist. In such [illegible] use, it [illegible] possible [illegible] realize without [illegible] heat sink or **** [illegible] like the [illegible]
[illegible] attained by either [illegible] following [illegible] when taken [illegible] method [illegible]

 3/2/03 [illegible]2

the heat sink member used as (1) object from a design, or an additional structural function like support of this member of the definition of the amount of capsule-like closure, or an MCM tile, in the structural member used as (2) objects, it is the method of replacing the high temperature conductivity metal (expensive [with copper] generally) which should originally be used for a heat sink by thermally conductive material like plastics (comparatively cheap).

[0030] In the latter use, without generating the cost which starts when realizing heat sink structure completely, the advantage of thin form mounting is maintained and it is rather strengthened as possibility.

[0031] Schematic drawing shows the example 10 of a changed completely type of an MCM package to drawing 1 . The PW board 11 which has much level sections consists of the lower level section 12, the central part level section 13, and the up level section 14. In this modification, while the lower level section 12 is continuation, as for the central part and the up level section, it has penetration opening respectively, and the gradual opening 15 is formed of these and this gradual opening forms the cavernous section 16 with the lower level section 12 by them.

[0032] In one example, an MCM tile is the silicon-on silicon MCM tile 17 which consists of a silicon substrate 18 and silicon chips 19 and 20, and is located in a cavity. A silicon substrate serves as a form which appeared in cavernous circles on the front face of the lower level section of PW board. The interconnection of the wire bond finger 21 on a silicon substrate is carried out to the contact pad 23 on the central part level section of PW board through a wire 22.

[0033] Through a breakthrough 24, it replaces, and interconnection is carried out to a contact 25, the interconnection of these pads is carried out to the solder bump 26 on the base of the lower level section by this, and interconnection is carried out to other chips or electron devices still like the signs 27 and 28 on the front face of the up level section of PW board as an option to other level sections of PW board.

[0034] which drawing of appending on these specifications -- also setting -- since it is easy -- **** -- although only few numbers of contacts and breakthroughs are illustrated, about these contacts on PW board, and the configuration method of a breakthrough, it is common knowledge technically The MCM tile which appeared on the front face of the lower level section is in the interior of the cavernous section 16 completely, and the upper surface of a chip is below the upper surface of the up level section of PW board.

[0035] The cavernous section 16 is filled up with a capsule-like sealing agent 29 like silicon gel which is highly adaptable. The capsule-like sealing agent 29 seals the interconnection section between the wires which interconnect a chip and a silicon substrate, the wire bond finger on a silicon substrate, the contact pad on PW board, and a wire bond finger and a contact pad.

[0036] The structural member 30 which works as a heat sink to a device 10 again, and seals the cavernous section is formed. The trailer 31 of a structural member (heat sink) appears on the up level section of PW board. Although the heat sink has kept the interval from the chip of an MCM tile, it approaches sufficient grade to incorporate the heat of a device generated by the component of an MCM tile working, and is located. thermally conductive adaptation like a thermally conductive paste or heat grease as an option -- a member 32 is formed so that a chip and a heat sink may be contacted physically

[0037] A schematic-drawing cross section shows another modification 35 of an MCM package to drawing 2 . The silicon-on silicon MCM tile is similar to the MCM tile 17 stated by drawing 1 . Therefore, the same sign is attached about this drawing 2 and the MCM tile from the following drawing 3 to drawing 10 . If explanation of drawing 2 is continued, the penetration opening 37 will be formed in the having-the single level section PW board 36.

[0038] It is arranged so that an obstruction 38 may be formed in the upper surface of PW board and the surroundings of opening may be revolved. From opening, an interval is kept and an obstruction is established so that the interconnection between a silicon substrate and PW board may be possible. An obstruction functions as a cage of the adaptability capsule-like sealing agent for wrapping in an MCM tile.

[0039] A structural member 39 is fixed to the base of PW board. A structural member is a rigid plate, and only in order to seal the edge of opening, it is used also as a heat sink. Plastics material is used for a structural member at the former purpose, and the other materials which have a metal or a high electric heat property are used for the latter heat sinks. The cavernous section 40 is formed of a structural member, the wall of opening, and the wall of an obstruction. The MCM tile 17 is in a cavity, and the silicon substrate 18 of an MCM tile appears on a structural member, and is in a structural member and a contact state.

[0040] The wire bond finger 21 on a silicon substrate is connected to the contact pad 41 on PW board by the wire 22. An MCM tile and the interconnection section are shape[of a capsule]-closed in the capsule-like sealing agent 29 of adaptability like silicon gel. Like drawing 1 , silicon gel wraps in the interconnection section between a substrate and a chip and between a substrate and PW board, and protects these interconnection sections from environment.

[0041] The device 35 by which interconnection was carried out electrically and mechanically to the mother board 42 at drawing 3 is shown. A mother board has the opening 43 of sufficient size to connote an obstruction 38, laps on PW board, and is electrically connected to PW board by solder or the interconnection section 44 of an electroconductive glue.

[0042] A schematic-drawing cross section shows still more nearly another modification 45 of an MCM package to drawing 3 . An MCM package consists of the MCM tile 17, a PW board 46 which has the two level sections, and a structural member 47 which acts as a heat sink. The gradual opening 48 which pierces through both the lower level section 49 of PW board and the up level section 50 is formed in PW board. The lower level section 49 of PW board appears on a structural member, and a structural member seals the end section of opening 48, and forms the cavernous section 51.

[0043] An MCM tile is located in the cavernous circle formed of the structural member and the wall of gradual opening, and the silicon substrate 18 of an MCM tile appears on a structural member. A wire 22 interconnects the wire bond finger 21 on a silicon substrate and the contact pad [illegible] level section of PW board.

[0044] In order that it may replace and the contact pad 52 may connect with another PW board or an another mother board in the future, interconnection is carried out to the contact pad 54 on the up level section 50 of PW board through a breakthrough 53. In addition, an MCM tile and the wire interconnection section are shape[of a capsule]-closed in the silicon gel 29.
[0045] The case where interconnection is carried out to drawing 5 electrically and mechanically at another board [like a mother board] 55 whose device 45 of drawing 4 is is shown. A mother board 55 laps with the up level section of PW board which has this two level section, and seals the cavernous section 51. A mother board 55 is connected to PW board by the solder reflow interconnection section 56.
[0046] It set by drawing 5 from drawing 1 , and the MCM package explained the case where it had the structure where the interconnection of the wire bond finger on the silicon substrate of an MCM tile is carried out to the contact pad on PW board by the wire.
[0047] Although nickel plating of the related pad on the wire bond finger made from the metal in which wirebonding like aluminum is possible in order to obtain effective interconnection, and PW board was carried out to copper, let it be the surface finish which is made by plating gold (gold and excess nickel plating) upwards and in which wirebonding is possible. By losing wirebonding interconnection, the need for expensive gold and excess nickel plating about the copper on PW board will also be lost.
[0048] The MCM package set and explained by drawing 10 from drawing 6 is manufactured without wirebonding between a silicon substrate and PW board. In this case, adhesion (bonding) is performed using the interconnection technology by the solder reflow or the electroconductive glue. In soldering, the contact pad of the pattern which is in agreement with the I/O (I/O) pad on an MCM tile is prepared in PW board by the known method.
[0049] In order to obtain the front face suitable for reflow solder, surface finish which grants respectively metallic coating which has the wettability to solder is performed to these contact pads by the known method. By this interconnection, the need for wirebonding for connecting the circuit on a silicon substrate to the circuit on PW board is lost.
[0050] In order to enable use of printing solder as an interconnection medium between an MCM tile and PW board, the wire bond finger 21 of the top from drawing 1 to drawing 5 (for example, an MCM tile substrate) or other wire bond fingers are replaced by the I/O metal pad which has the wettability to solder to which condensation adhesion (deposit) was carried out simultaneously with an interconnection flip chip MCM pad.
[0051] In one example, the I/O metal pad which has the wettability to these solder is formed as a 96micrometerx146micrometer pad at intervals of a 305 micrometers (12 mils) pitch so that it may be possible to print the deposit of 170micrometerx280micrometer soldering paste as soon as soldering paste is printed on the internal I/O pad used in order to attach a chip in a substrate.
[0052] This process is applied to producing the MCM tile which prepared the solder bump using inside like 95/5 Sn/Sb, or high-melting point solder. On an MCM tile, after the assembly of a wafer, washing, inspection, and the division into each tile are completed, a solder bump is prepared in each output pad on each tile. These pads are suitable for performing reflow soldering by printing eutectic (or ******) Sn/Pb soldering paste common to the assembly by the standard surface mount technology in itself.
[0053] Incidentally, yield (that is right when a die with a solder bump is examined electrically like) also improves by adding a solder bump to the I/O pad of an MCM tile by reducing the number of the excellent article tiles which the good testability improved, therefore were refused by misreading.
[0054] The technology for forming a solder bump on the metal pad of an element like an IC package, a substrate, or PW board is indicated by U.S. Pat. No. 5,346,118 (September 13, 1994 issue). Let this U.S. patent be the bibliography of this application here. In case this solder bump formation technology manufactures a device, without using the interconnection by wirebonding, it is very useful.
[0055] An MCM tile shows the MCM package 60 by which interconnection was carried out with solder bonding at PW board to drawing 6 with schematic drawing. This MCM package has PW board which has the two level sections which consist of the lower level section 62 and the up level section 63. The gradual opening 64 opened on the base of the lower level section of PW board is formed in PW board.
[0056] The size of the gradual opening 64 is the size to which the chip on a silicon substrate is restored to opening of lower level circles, without being suitable caudad and contacting the wall of opening, while the edge of a silicon substrate laps on PW board field which adjoins opening of lower level circles of PW board, when the interconnection of the silicon substrate of an MCM tile is electrically carried out to PW board.
[0057] The physical relationship of the MCM tile 17 is the physical relationship which is in the position where chips 19 and 20 turned to the lower part in opening of the lower level section, and the chip moreover retreated from the base of the lower level section of PW board to the inner direction of opening, while the upper surface of the silicon substrate 18 of an MCM tile turns to the upper part. A structural member 65 adjoins a silicon substrate and is prepared in a device 60 again. This structural member seals the end section of opening, and defines the cavernous section 69 with the wall of opening 64. A structural member is made from high temperature conduction material, and is used as a heat sink to an MCM tile.
[0058] The bond finger 67 on a silicon substrate is electrically connected to the contact 68 on PW board by the solder reflow interconnection section 69. The cavernous section is filled up with the silicon gel 29, and this silicon gel seals and protects the interconnection section between the bond finger between a chip and a silicon substrate, on a silicon substrate, and the contact on PW board.
[0059] [illegible] edge [illegible] substrate contacts the [illegible] on PW board the [illegible]

the solder interconnection section and a chip has it in opening, the thickness of an assembly is cut down by even the thickness of PW board. if it contrasts with the thickness of the MCM tile-on and "PW board" assembly resulting from having mounted the MCM tile [as / in the Prior art illustrated by drawing 11 and drawing 12 in this] on the crowning of PW board, having turned the chip up, and having carried out wirebonding to the circuit of PW board, the dominance which is this example is clear

[0060] An MCM tile shows another MCM package 70 by which interconnection was carried out with solder reflow bonding at PW board to drawing 7 with schematic drawing. An MCM package has PW board which consists of the single level section, and the penetration opening 72 is formed in PW board. While the physical relationship of the MCM tile 17 has the chips 19 and 20 of an MCM tile in opening 72, it is the physical relationship which is in the position where the edge of the silicon substrate 18 of an MCM tile laps with the base of PW board which adjoins opening so that a silicon substrate may come to the outside of opening.

[0061] The bond finger 73 on a silicon substrate is electrically connected to the contact 74 on PW board by solder reflow interconnection. While the cup-like covering 75 contacts the base of a silicon substrate, the edge flange 76 of covering is attached in the pars basilaris ossis occipitalis of PW board by adhesives (not shown). Cup-like covering is made from the plastics which has a metal like copper, or a high temperature conduction property, in order to use as a heat sink to an MCM tile. In metal covering, there is an advantage of acting as a cover object over electromagnetic radiation.

[0062] The cavernous section 77 is formed by the wall and cup-like covering of opening 72, it fills up with an adaptable capsule-like sealing agent like silicon gel partially, and this sealing agent seals and protects the interconnection section between an MCM tile and a bond finger, and a contact.

[0063] The case where interconnection is carried out to drawing 8 electrically and mechanically at another board [like a mother board] 78 whose device 70 of drawing 7 is is shown. A mother board 78 is located in the upper surface of PW board, laps with the cavernous section 77, and is electrically connected to PW board by the solder reflow interconnection section 79.

[0064] Schematic drawing shows another modification 80 of a semiconductor package in case the interconnection between an activity semiconductor device and PW board is obtained by the solder reflow by drawing 9 . However, in this modification, the interconnection of a sign 81, a single like 82, or two or more chips of each is carried out to the PW board 83 which has the two level sections of the lower level section 84 and the up level section 85 by the solder reflow instead of an MCM tile. Opening 86 is formed in the up level section of PW board.

[0065] A chip is located in the cavity formed of the lower level section of PW board, and the wall of opening 86. In order that two or more heat sink insertion objects 88 (known also as ****) may remove heat from a chip, it is prepared in the lower level section of PW board. The cavernous section is filled up with an adaptability **** capsule-like sealing agent 29 like silicon gel, and this sealing agent seals and protects the interconnection section between a chip and PW board.

[0066] The case where it connects with drawing 10 electrically and mechanically at another board [like a mother board or other PW boards] 89 whose device 80 of drawing 9 is is shown. A board 89 laps on the up level section of PW board, and interconnection is carried out to the PW board 83 by the solder reflow interconnection section 90.

[0067] Finally, when PW board is the middle interconnection or leadframe board mounted on a leadframe PW board by analogous and the mother board (either an one side flexibility PW board or a double-sided rigidity PW board), PW board is patternized so that the I/O array (array) of the solder pad which followed strongly the bump (heights) in whom solder printing is possible may be suited. Although the solder pad with a bump has an advantage, a pad without a solder bump is not excepted from this invention, either.

[0068] For example, it is possible by using a 1.52mm (60 mils) OMPAC standard BGA pitch to form easily the circumference array which two solder pads with a diameter of 0.71mm (28 mils) leave and which is and consists of a difference train. In this case, the total of the I/O pad in a 25.4mmx25.4mm package is set to 108. (In order to make wiring routing easy, a pile difference train method is used also in a cheap one side PW board)

[0069] Room space required for opening of (1) (2) tile is obtained with many I/O nodes of 108, without changing which configuration or size of a zone on the mother board which is needed for the interconnection of an MCM package or the following level section by this. Simultaneously, in addition, the strong attachment to the mother board of a printing solder BGA bump and surface mounting reflow solder is possible.

[0070] The further additional advantage about this invention and the way of thinking of change are easy for the above explanation to this contractor about one example of this invention. Therefore, the mode of this invention is not limited to the specific example of a detailed representation device described above. Therefore, although the various modifications of this invention can be considered, each of they is included by the technical range of this invention.

[0071] For example, the structural member shown in some examples like the structural member shown as the sign 30 of cup-like covering shown as a sign 75 of the structural member shown as a sign 47 of the sign 39 of drawing 2 and drawing 3 , drawing 4 , and drawing 5 or drawing 7 , and drawing 8 or drawing 1 and a sign 65 of drawing 6 does not necessarily need to be a heat sink, and does not interfere by mere reinforcing materials or supporter material.

[0072] In not working as a heat sink, it manufactures all of these structural members from non-thermal conductivity like plastics material, or low-fever conductivity material. In a certain case, you may completely lose structural members 30 and 65.

[0073]

[Effect of the Invention] As stated above, according to this invention, in a multi-chip module (MCM) package, it becomes possible [illegible] preparing the cavern[illegible] sec[illegible] a printed [illegible] (PW) [illegible] and arranging an MCM tile efficiently to obtain the package [illegible] down the per[illegible] [illegible] thic[illegible] [illegible] with the MCM package by the conventional technol[illegible] [illegible] since the [illegible] was [illegible] suitable [illegible] fusion of ge[illegible] [illegible]

a chip, such as a heat sink, it can respond also to high-power density specification easily in a thin form.
[0074] Therefore, it can respond to the need of the package miniaturization to which a demand becomes strong increasingly, and the miniaturization of the system and equipment which adopt a package is attained.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is a semiconductor device and this device is an outline cross section in the case of consisting of an MCM tile mounted on PW board which has the level section of a large number which have gradual opening. In this device, the MCM tile located in the cavernous circles formed on PW board is electrically connected to PW board by wirebonding, a structural member seals the cavernous section, and it fills up with the adaptability capsule-like sealing agent which wraps in the chip of an MCM tile at least in the cavernous section.

[Drawing 2] It is a semiconductor device and this device is an outline cross section in the case of consisting of a PW board which has the single level section which has gradual penetration opening defined by the wall of PW board, and the wall of an obstruction located on PW board. In this device, a structural member is attached in PW board, the end section of opening is sealed, a structural member, the wall of opening, and the wall of an obstruction form the cavernous section, an MCM tile is located in the cavernous circles on a structural member, and it fills up with the adaptability capsule-like sealing agent with which wirebonding connects with PW board electrically, and an MCM tile wraps in an MCM tile in the cavernous section.

[Drawing 3] In the semiconductor device shown in drawing 2 , it is an outline cross section in case a mother board is electrically connected to PW board.

[Drawing 4] It is a semiconductor device and this device is an outline cross section in the case of consisting of a PW board which has the two level sections which have gradual penetration opening. In this device, a structural member is attached in PW board, the end section of opening is sealed, a structural member and the wall of opening form the cavernous section, an MCM tile is located in structural-member absentminded sinus circles, and it fills up with the adaptability capsule-like sealing agent with which wirebonding connects with PW board electrically, and an MCM tile wraps in an MCM tile in the cavernous section.

[Drawing 5] In the semiconductor device shown in drawing 4 , it is an outline cross section in case the mother board electrically connected to PW board is located in the MCM tile upper part and seals the cavernous section.

[Drawing 6] It is a semiconductor device and this device is an outline cross section in the case of consisting of a PW board which has the two level sections which have gradual penetration opening. In this device, an MCM tile is mounted on the cavernous circles formed of the gradual wall of opening. An MCM tile is electrically connected to the lower level section of PW board through the interconnection by the solder reflow or conductive adhesives. The cavernous section is filled up with the adaptability capsule-like sealing agent which wraps in an MCM tile, and the cavernous section which a structural member is arranged in the shape of [of the substrate of an MCM tile / upper] a PW board, and has it in a substrate side is sealed.

[Drawing 7] It is a semiconductor device and this device is an outline cross section in the case of consisting of a PW board which has the single level section which has penetration opening. In this device, while the interconnection of the substrate of an MCM tile is electrically carried out to the pars basilaris ossis occipitalis of PW board through the interconnection by the solder reflow or conductive adhesives The chip of an MCM tile is located in opening, and above an MCM tile, cup-like covering contacts a substrate and is arranged. The flange edge of cup-like covering contacts PW board, cup-like covering and the wall of PW board form the cavernous section, and it fills up with the capsule-like sealing agent which has adaptability in the cavernous section.

[Drawing 8] In the semiconductor device shown in drawing 7 , it is an outline cross section in case the mother board electrically connected to PW board by the cup-like covering and opposite side is located in the MCM tile upper part and seals the cavernous section.

[Drawing 9] It is a semiconductor device and this device is an outline cross section in the case of consisting of a PW board which has the two level sections which have opening in the up level section of PW board. The cavernous section is defined by the lower level section and the wall of the up level section in this device. Two or more heat sink fields are located in the lower level circles of PW board through this lower level section. It connects with a heat sink field thermally, and two or more silicon chips located in the lower level section absentminded sinus of PW board are electrically connected to PW board by a solder reflow or conductive adhesives, and it fills up with the capsule-like sealing agent which has adaptability in the cavernous section.

[Drawing 10] In the semiconductor device shown in drawing 9 , it is an outline cross section in case it connects with the up level section of PW board electrically and a mother board seals the cavernous section.

[Drawing 11] It is the outline cross section of the OMPAC device by the conventional technology which has the interconnection by wirebonding between semiconductor tile chip and PW board.

[Drawing 12] It is the outline cross section of another device by the conventional technology which interconnected the MCM tile by wirebonding.

[Description of Notations]
10, 35, 45, 60, 70 Modification of a multi-chip module (MCM) package
11 Printed Wiring (PW) Board Which Has Much Level Sections
12 Lower Level Section
13 Central Part Level Section
14 Up Level Section
15 Gradual Opening
16 Cavernous Section
17 Silicon-on Silicon MCM Tile
18 Silicon Substrate
19 20 Silicon chip
21 Wire Bond Finger
22 Wire
23 41 Contact pad
24 Breakthrough
25 Contact
26 Solder Bump
27 Other Electron Devices
28 Other Chips
29 Capsule-like Sealing Agent (Silicon Gel)
30 Structural Member
31 Trailer of Structural Member
32 Thermally Conductive Adaptation -- Member
36 71 PW board which has the single level section
37 72 Penetration opening
38 Obstruction
39, 47, 65 Structural member
40, 51, 66, 77, 87 Cavernous section
42, 55, 78, 89 Mother board
43 Opening (Mother Board)
44 Solder or Interconnection Section of Electroconductive Glue
46, 61, 83 PW board which has the two level sections
48 Gradual Penetration Opening
49, 62, 84 Lower level section
50, 63, 85 Up level section
52 54 Contact pad
53 Breakthrough
56, 69, 79, 90 Solder reflow interconnection section
64 Gradual Opening
67 73 Bond finger
68 74 Contact
75 Cup-like Covering
76 Edge Flange
80 Semiconductor Package
81 82 Chip
86 Opening
88 Heat Sink Insertion Object (****)
100 120 Typical example of the ball grid array (BGA) package of an exaggerated mould plastics pad array carrier (OMPAC) (device)
101 IC Unit
102 125 PW board
103 126 Wire bond finger
104 Polymer Coating
105 128 Breakthrough
106 129 Contact pad
107 130 Wire
108 Molding Compound
109 133 Solder ball
121 Mo[illegible]
122 12[illegible]

124 Silicon Interconnection Substrate
127 Solder Mask
131 Protection Shell
132 Capsule-like Sealing Agent

[Translation done.]

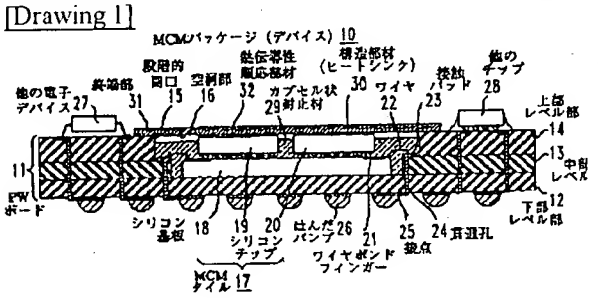
* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

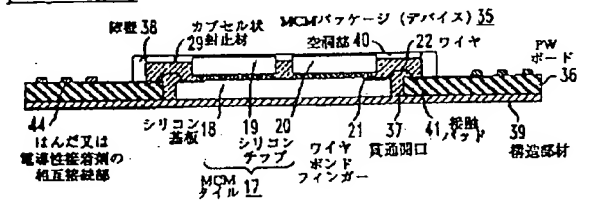
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

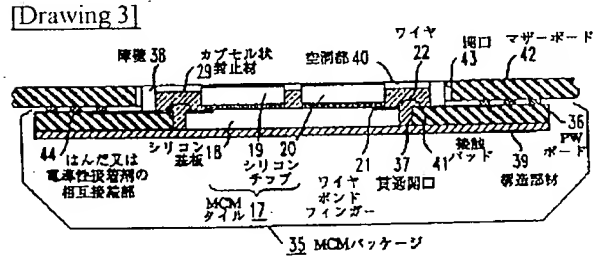
[Drawing 1]



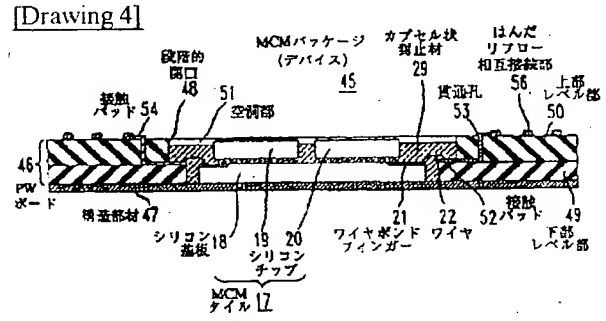
[Drawing 2]



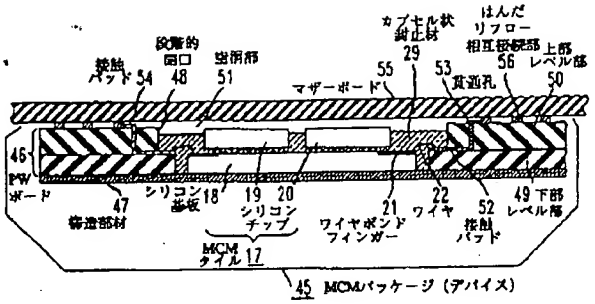
[Drawing 3]



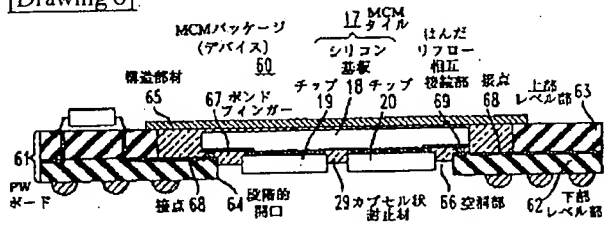
[Drawing 4]



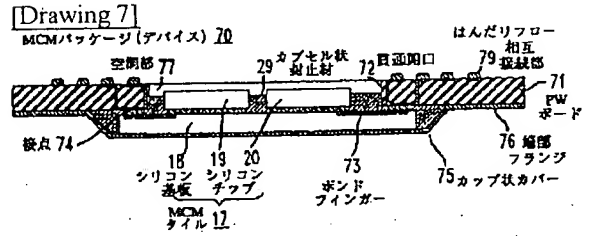
[Drawing 5]



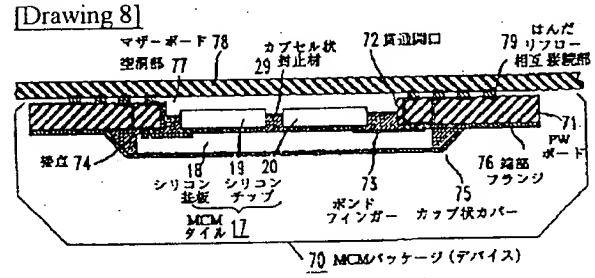
[Drawing 6]



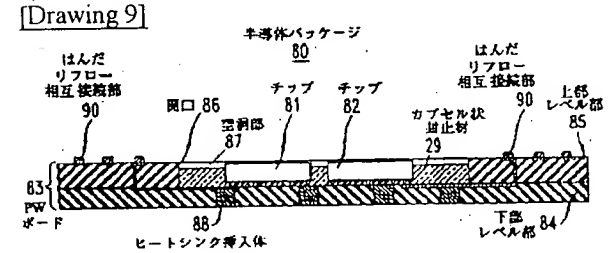
[Drawing 7]



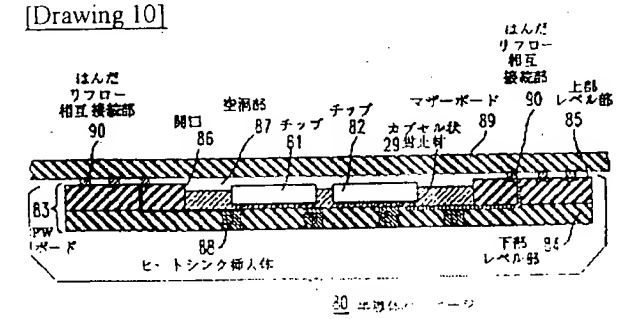
[Drawing 8]



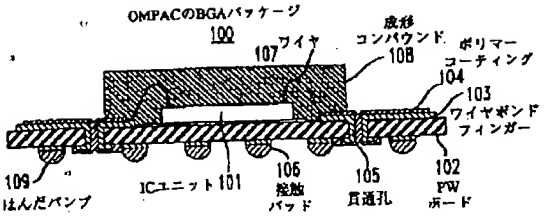
[Drawing 9]



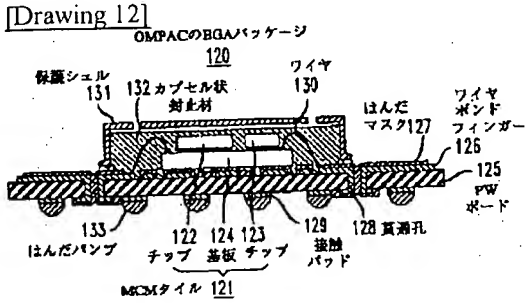
[Drawing 10]



[Drawing 11]



[Drawing 12]



[Translation done.]